(Invited)

THE FUTURE OF RFIC TRANSCEIVER TECHNOLOGY

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Abstract

RFIC Technology is still in the infancy phase. The requirement for extremely low-cost, high-performance RF transceivers will drive dramatic changes in system architecture, semiconductor technology, and circuit implementation in the next few years.

This paper addresses some of these issues and presents results that illustrate new directions in RFIC transceiver technology development.

1. Introduction

New systems for digital mobile communications operating in the 800MHz to 2GHz band, such as GSM, PHS, DECT, and CDMA are being deployed at a rate which far exceeds the deployment rate of any other consumer product ever introduced. As an example GSM has been adopted by more than one hundred operators over the world (in about fifty countries); and it is expected that 30 million handsets will be sold in 1997, up from 15 million in 1996.

The Bill of Material of these handsets drops about 30% every year while the demand for better performance (speed, power consumption) and functionality (voice/data service, multi-standard, multi-band) is increasing. The cost and performance of digital CMOS technologies driven by the requirement of the computer industry are responding to this demand. However, RF IC technologies are still in the infancy phase.

Optimum architecture, high level of integration, low voltage (below 3V) and efficient hardware/software signal processing will require dramatic architecture, semiconductor technology, and circuit implementation changes in the next few years.

This paper addresses some of these issues and presents results that illustrate the trends and options in developing RF/IF IC components for wireless communications.

2. RF Architecture

2.1. Transceivers

The transceiver architecture ultimately defines the handset performance, cost, and manufacturability. It includes 1) the analog and mixed-signal functions of the physical layer, 2) the interfaces with the equalizer and the data receiver (demodulation, carrier recovery...), 3) the interfaces with the control, calibration and resource management software functions, and 4) the interface with the power management functions.

The RF transceiver architecture can be hardware or software intensive. Hardware transceivers are mainly based on a narrowband architecture, using analog filters, and are generally developed to address specific applications or standards. Software transceivers are based on a wideband architecture using a combination of analog "roofing" filters and digital programmable filters for signal channelization. The physical layer of software radios is, in principle, designed to be standard independent.

All the cellular phones and base station transceivers are currently based on hardware architectures, but it is expected wideband software architectures are to be implemented in "programmable" base stations in 1997/1998.

2.2. Receivers

Most of the transceivers currently in production are still based (as shown in Figure 1) on a double- or single-down conversion receiver followed by an A to D converter, FIR filters, an equalizer/ demodulator, and a single up-conversion transceiver followed by a D to A converter and its reconstruction filter. This architecture is somewhat costly due to its high component count as well as to the need for several expensive external filters. However, it has proven to be extremely manufacturable.

Two other architectures are aggressively pursued to reduce the cost of existing radios and, as important, to provide a path for multi-standard radio development: the direct conversion/zero IF architecture [1] and the single IF undersampling architecture [2].

In the direct conversion/zero IF solution (Figure 2), filtering and analog processing are performed at baseband and as such does not require expensive and cumbersome RF filters or high-frequency processing functions. It suffers, however, from low sensitivity due to base band noise contribution, the requirement for extremely low LO leakage at the antenna in the receive mode (LO acts as an interferer since it operates at the same frequency as RF signal), the need for very high linear mixers, and a large DC offset contribution due to self-converting LO and near-channel interferer to DC. Despite extensive efforts from numerous design teams, these issues have not been resolved yet.

The single IF undersampling architecture (Figure 3) virtually eliminates the zero IF design issues but requires a high-frequency, high-dynamic range A to D converter [3] [4].

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ADCs providing over 90dB SFDR at 200 MHz IF and 60MSPs are now available and will enable narrowband or wideband IF sampling solutions for base station applications and later for handset/pager applications. IF and baseband processing are digitally performed in hardware or software form. This approach drastically reduces complexity and cost of the multi-channel radio receivers.

3. Technology

New silicon bipolar IC processes tailored for low-voltage, low-power consumption RF and mixed-signal applications have reached the performance and cost required for mass production of RF transceivers operating in the 1 to 2GHz frequency range. GaAs, which initially was the only contender at frequency above 2GHz, will be very much challenged by small geometry silicon ICs in their homojunction or heterojunction (SiGe HBT) form.

Table 1 summarizes the performance of competing technologies addressing RF IC applications. It can be seen that silicon technology compares extremely well with GaAs in terms of performance with the advantage of providing an existing low-cost, high-volume production base.
Missing in this table is submicron low-voltage CMOS technologies, which with F_T and F_{max} in excess of 10GHz, less than 2dB noise figure at 2 GHz and excellent linearity have already demonstrated good performance up to 2GHz [5]. Further technology refinement (low threshold voltage, low gate and source contact resistance, thick metalization...) will make CMOS extremely competitive for RF applications in the next few years.

4. Applications

This section presents two alternative RF IC solutions for DECT cordless phones and a generic solution for wideband base stations.

4.1. DECT

4.1.1 Narrowband Double Conversion

Figure 4 shows the block diagram of an RF transceiver chipset developed at Analog Devices for DECT (Digital Enhanced Cordless Telephone). DECT operates at 1.9GHz in a TDMA/TDD mode and uses 10 frequency channels spaced 1.728MHz apart. Each frequency is divided in 24 time slots (12 receive/12 transmit) receiving and transmitting GFSK (Gaussian Frequency Shift Keying) modulated signal at a 1.152 Mbit/s data rate.

A 25GHz F_T junction-isolated silicon-bipolar process is used to fabricate the RF chip, and a 5GHz SOI (Silicon on Insulator) silicon complementary bipolar process is used for the IF chip.

The two chips included all the RF/IF functions and also voltage regulators, ESD protection diodes, and power management logic circuitry. They can operate from 2.7 to 5V.

The RF chip includes a Rx and a Tx mixer, a VCO, a buffer, and a driver amplifier. The IF chip includes a Rx mixer covering the first 110MHz IF frequency down to 20.7MHz, a PLL demodulation loop, which outputs a 1.1MHz signal to a 6 bit A to D converter, and an IF VCO providing 131 MHz GFSK modulated signal to the RF chip.

The two RF/IF chips together with the baseband interface and DSP unit achieve a -94dBm sensitivity level for a 10^{-3} BER (DECT specification is -83dBm) and provide 0dBm pulsed output power compliant with the DECT spectrum and switching transient mask. As an example Table 2 shows the RF receive chain performance.

4.1.2. Wideband Double Conversion

A competitive approach based on a single chip 0.6μm CMOS DECT receiver including an LNA, an image reject mixer, two baseband filter and two 10b ADCs has been proposed in [6]. The receiver is based on a wideband double conversion architecture. Channel selection is done in baseband using gmC and switched-capacitor filters. The receiver provides -90dBm sensitivity and proves RFCMOS technology is "just around the corner."

4.2. Wideband Programmable Receiver

An IF sampling 900MHz receiver using digital channelization and exhibiting over 80dB dynamic range will be presented at the conference.

5. Conclusion

The RF IC technology is evolving very rapidly. It has already enabled RF transceivers to meet the stringent requirements for high-performance, high-volume, low-cost consumer applications.

RF ICs are the critical components of the terminal hardware. They process the signal coming from the terminal antenna and deliver bits to the digital data receiver.

The need for low-cost, low-voltage, low-power consumption ICs are pushing the designers towards new architectures and new semiconductor processes as well as high levels of integration. The RF technology is no longer an "esoteric" and marginal technology. It is the technology that will ultimately allow for the development of 1) extremely low-cost "hardware" wireless transceivers on one hand, and 2) highly programmable "software" terminals on the other hand.

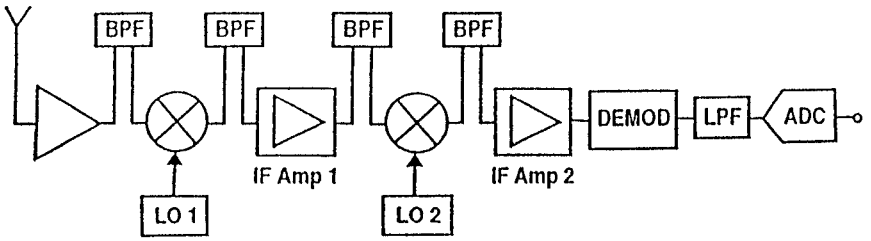

Figure 1. Double Conversion Receiver

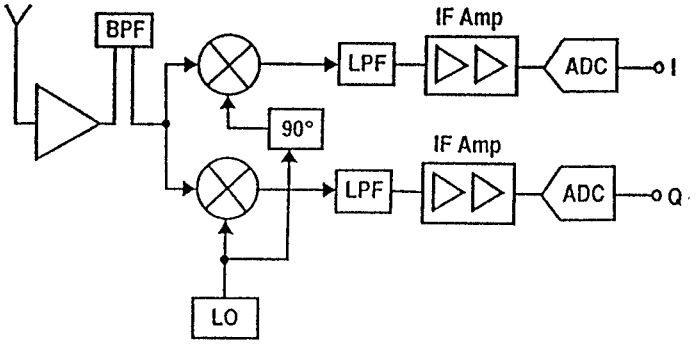

Figure 2. Direct Conversion Receiver

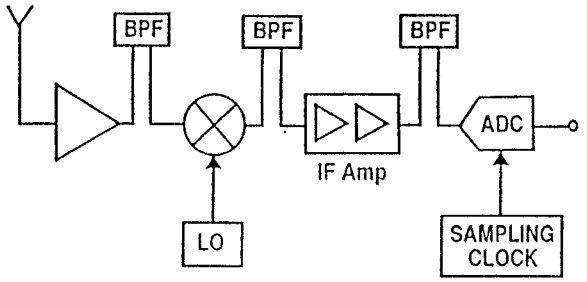

Figure 3. Direct IF Sampling Receiver

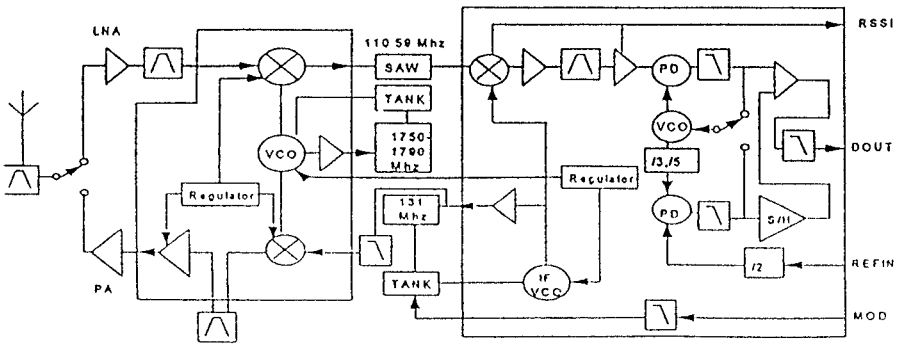

Figure 4. DECT RF IC Block Diagram

	SiGe HBT	SiBJT	AlGaAs/ GaAs Hbt	GaAs MESFET	SiBJT BiCMOS
Minimum size (μm)	0.5 x 1	0.5 x 1	2 x 5	0.5 x 5	1.2 x 1.5
BV_{CEO}/BV_{DS} (V)	4	4	15	8	6
f_t (GHz)	50	32	50	30	13
f_{max} (GHz)	55	35	70	60	11
G_{max} (dB) @ 2GHz	28	24	19	20	17
@ 10 GHz	16	11	13	13	1
F_{min} (dB) @ 2GHz	0.5	_	1.5	0.3	_
@ 10 GHz	0.9	_	_	0.9	_
IP_3/P_{1dB} (dB)	9	9	16	12	9
P_{add} Efficiency (%) @ 3V	70	_	60 @ 5v	70	40
1/comer (KHz)	0.1-1	0.1-1	1-10	10,000	0.1-1

Table 1. Comparison of key figures of merit for five processes

Rx Mixer	Performance		Specification		Unit 1A
					Measured
	Conversion gain		8 to 12		11.7
	SSB Noise Figure		15		14
	RF RL		-15		-15
	IF RL		-15		-25
	i/p P1dB		-12		-14
	IIP3		-3		-5.2
	LO Leak	at RF	-24		-31
		at IF	-19		-32.8
	RF-IF ISO		10		41
	Spurious	RFx2LO	-28		-44
		2RFx2LO	-50		-72
		3RFx3LO	-36		-44
		RFx3LO	-44		-68

Table 2. DECT RF IC receive chain performance

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